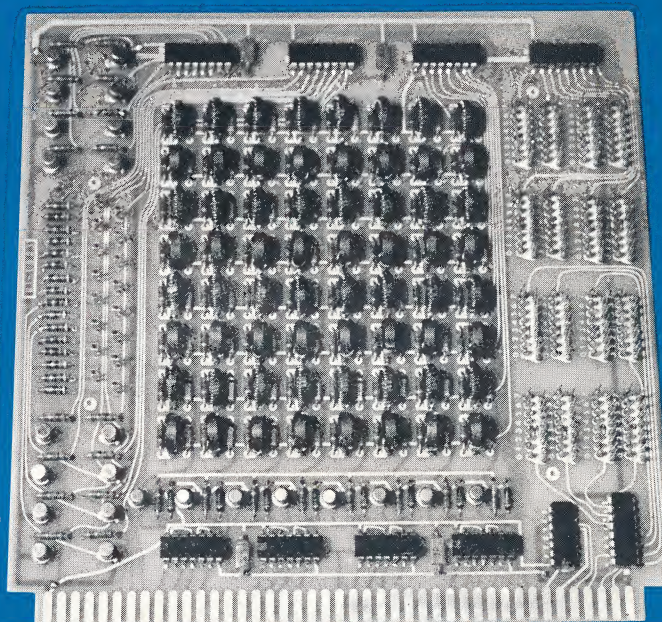


LOW COST READ ONLY MEMORY

UI-1003

RUGGED CONSTRUCTION - HIGHEST RELIABILITY

- LOWEST COST
- 350 nS CYCLE TIME
- 5 VOLT POWER SUPPLY
- SIZE: 7-5/8" x 7-1/2" x 3/4"
- COMPATIBLE WITH TTL
- 8-BIT DATA REGISTER INCLUDED
- AVAILABLE IN SMALLER CAPACITIES
- STANDARD 2048 WORDS, 8 BITS/WORD
- PROGRAM EASILY ALTERED
- 14 DAY DELIVERY



ROM BOARD READY FOR CUSTOM BRAIDING

DESCRIPTION: The UI-1003 is a low cost, high speed transformer type Read-Only Memory designed with reliability and program alterability in mind. It includes address decoding, core matrix, and output data registers. It is TTL (74 series) compatible and uses a 5 volt supply. Incorporating state-of-the-art MSI circuits, it has a 350 NS read cycle time. Use of toroidal cores insures an uninterrupted magnetic path resulting in a rugged, reliable memory.

There is also available a low cost 256 x 8 ROM identical to the UI-1003 in every detail except size, it is 7-5/8 in. x 4 in. x 3/4 in. It is ideal in code conversion and character generation applications. Ease of memory changeability and 14 day delivery make it attractive as a breadboard or pre-MOS memory. Other word size memories are available and a special department is ready to discuss custom memory requirements.

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SYSTEM SPECIFICATIONS

Cycle Time 350 nanoseconds
Access Time 175 nanoseconds
Capacity Variable word and bit length up to
2048 words, 8 bits/word

INPUT SIGNALS — TTL74 Series Compatible

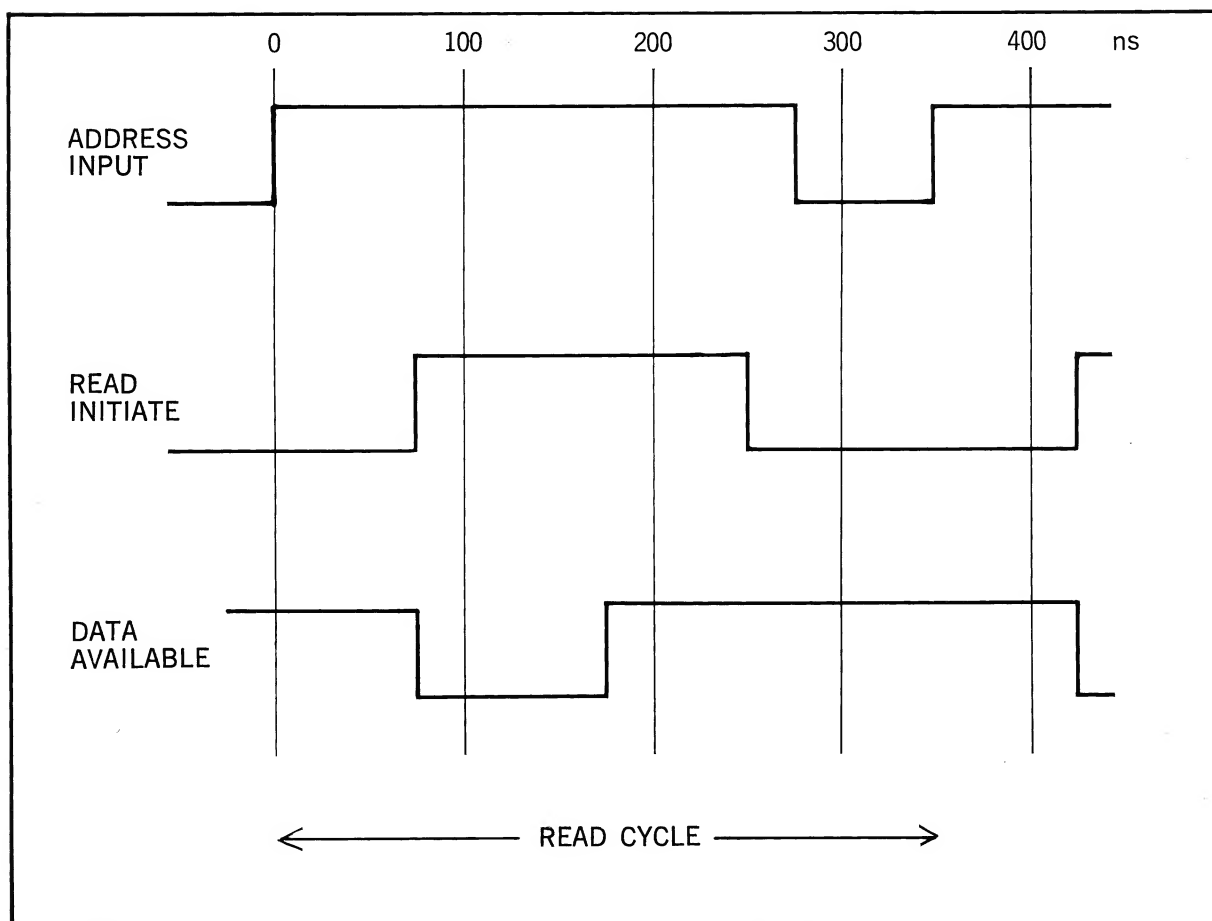
Logic "0" Maximum 0.4V
Logic "1" Minimum 2.4V
Address Up to 11 lines, Single Rail
Cycle Initiate 1 line

OUTPUT SIGNALS

Logic "0" Maximum 0.4V at 16 ma.
Logic "1" Minimum 2.4V
Data Up to 8 bits, Dual Rail, 16 lines
true and complement available

Power Supply Requirements $5V \pm 5\%$ at 500 ma.
Operating Temperature Range $0^{\circ}C$ to $55^{\circ}C$
Mechanical Dimensions $7\frac{5}{8}$ in. x $7\frac{1}{2}$ in. x $\frac{3}{4}$ in.
Plugs into 86 pin connector (156 mil centers)

READ/ONLY MEMORY TIMING DIAGRAM



UNICOM INC

WORLD'S LOWEST PRICED COMPUTER FAMILY

Starting at **\$1800**

**Quantity
Discounts**



CP-8 FAMILY FEATURES

- 1.5 MICROSECOND CYCLE TIME
- SET OF 50 BYTE VARIABLE INSTRUCTIONS
- UNIQUE DUAL MODE I/O INSTRUCTION SET
- CONTROL OF 1024 I/O DEVICES
- 4 PRIORITY INTERRUPTS
- UP TO 16 SCRATCHPAD REGISTERS
- 1-32K BYTES OF READ/WRITE MEMORY
- 0.5-4K BYTES OF READ ONLY MEMORY
- 2's COMPLEMENT ARITHMETIC WITH LINK

THE CP-8 FAMILY INCLUDES:

- CP-8A, CP-8B CONTROL PROCESSORS
- CP-8C GENERAL PURPOSE PROCESSOR
- CP-8D GENERAL PURPOSE PROCESSOR
WITH MAG TAPE CASSETTE STORAGE

CP-8 FAMILY APPLICATIONS

- PROCESS CONTROLLER
- INSTRUMENTATION CONTROLLER
- DATA CONCENTRATOR
- PERIPHERAL DEVICE CONTROLLER
- GENERAL PURPOSE COMPUTER
- EDUCATIONAL COMPUTER
- BIOMEDICAL COMPUTER
- TEST SYSTEMS
- ACCOUNTING SYSTEMS

COMPLETE READ/WRITE AND READ ONLY
MEMORY INTERCHANGEABILITY ALLOWS FOR
RAPID IMPLEMENTATION OF FIXED PROGRAM
LOW COST CONTROLLERS.

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INTRODUCTION

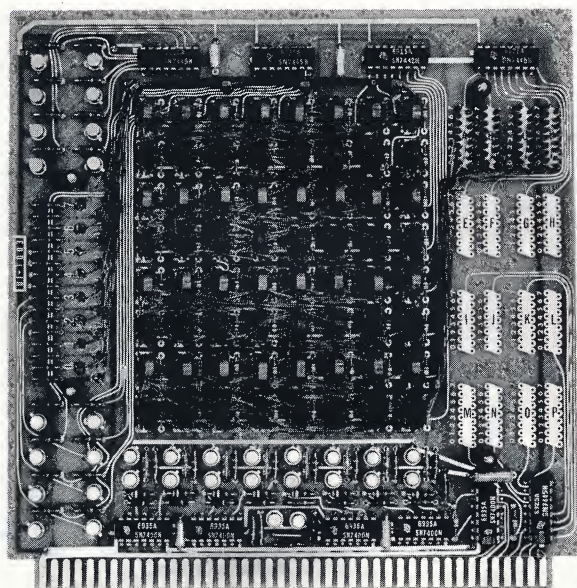
The CP-8 Family of compatible processors was conceived to provide maximum data handling capability and unprecedented flexibility at a minimum cost. The long recognized need for a truly basic, low cost, ROM-based processor-controller has been satisfied with the CP-8A and CP-8B. The CP-8C offers powerful processing and Input/Output capability for front end as well as general purpose applications. The CP-8D includes a cassette magnetic-tape mass storage system in addition to the main frame. All processors feature a 3.5 microsecond add time (1.5 microsecond memory cycle time) up to 50 basic commands, a hardware index register, priority interrupts, powerful I/O commands capable of handling 1024 external devices, and unique hardware flexibility. A modular plug-in design allows for expansion to include a full complement of options.

The use of proven TTL MSI circuitry assures maximum reliability and economy.

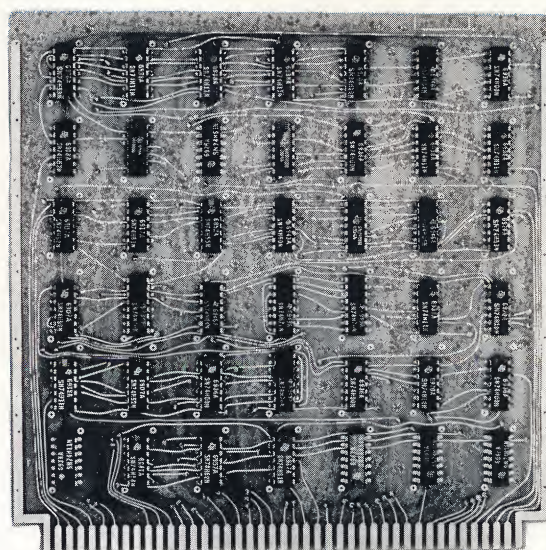
An off-the-shelf line of peripheral equipment is available at attractive prices. Special purpose equipment and interface circuitry can be developed to customer specification in minimum time.

MEMORY UTILIZATION

Since the memory represents a large portion of the total cost of the system, proper memory utilization is of major importance. The CP-8 family features unparalleled memory efficiency. Through the use of an unique paging-indexing method most commands can be controlled with an 8 bit code, resulting in high memory utilization. This feature is of major importance if a low cost fixed program controller is to be utilized in place of special purpose logic design, and if relative economy is a consideration.



READ ONLY MEMORY



BASIC PROCESSOR BOARD

THE CP-8 COMPUTER FAMILY

The CP-8 computer line is a compatible family of 4 basic computers. They are parallel, binary, fixed point, 2's complement machines with link capability, featuring an instruction set of up to 50 basic commands and a complete interchangeability of Read-Write Memory, Read-Only Memory and General Purpose Registers. It is the most flexible computer family available today.

CP-8A

This versatile digital controller is easily adaptable to system interfacing requirements. It features a basic processor, 4 General Purpose Registers and 512 bytes of Read-Only Memory (expandable to 4096 bytes). Eliminating the display panel and power supplies allows the user to incorporate the CP-8A within his own product at an overall cost saving.

CP-8B

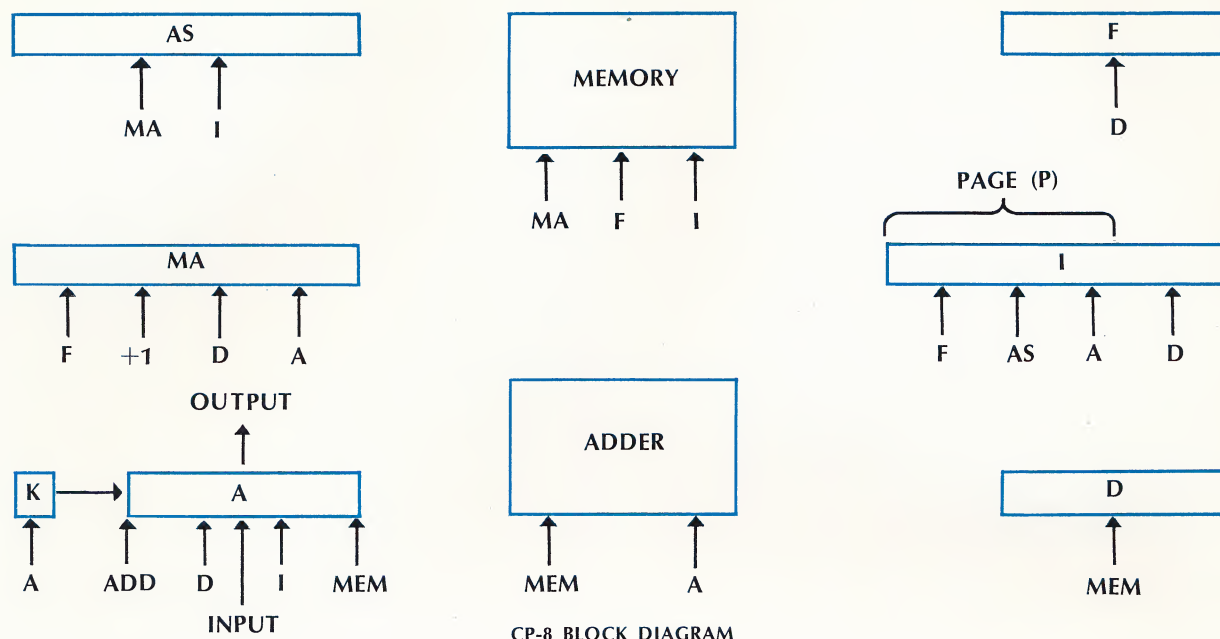
This controller features the basic processor, 16 General Purpose Registers, 512 bytes of Read-Only Memory (expandable to 4096 bytes) and 4 standard priority interrupts.

CP-8C

This mini-processor features 1024 bytes of Read-Write Memory (expandable to 4096 bytes), 1 index register, 4 interrupts, the basic processor, a display panel and 3 power supplies. This model is particularly useful when programs must be debugged in Read-Write Memory before being committed to Read-Only Memory. The CP-8C is also sold without the Read-Write Memory, thus permitting the customer to use any other available memory, if he so desires.

CP-8D

This is the only known mini-processor with mass storage available today. The Magnetic Tape Cassette Transport has a one million byte storage with full search capability. The timing, error detection and the tape control functions such as read, write, search and stop are internally controlled, and the user simply writes his program using the code of the desired function. The CP-8D also includes the basic processor, 4 priority interrupts, 1 index register, a display panel and 3 power supplies. 1024 bytes of Read-Write Memory is also available.



INPUT/OUTPUT FEATURES

All CP-8 family processors include a dual mode I/O system. The first mode is intended for peripheral device control, and the second for high speed asynchronous interfacing with other computers. This I/O capability allows the CP-8 to present itself as a peripheral device to the main CPU while simultaneously controlling a number of external devices. This feature is attractive in the data concentrator and front end applications. In the asynchronous mode, an input or output request is sent to the main CPU by the CP-8. The CP-8 then waits for an acknowledge signal. When the signal is received, the information transfer takes place in less than 100 nanoseconds. An eight bit device code allows selection of up to 512 external devices on both input and output asynchronous channels. In the conventional I/O mode the CP-8 tests for a peripheral device request. If the request is present, information is transferred and the device is acknowledged. If the request is not present other tasks are performed. Up to 512 peripheral devices can also be selected with that command.

HARDWARE FLEXIBILITY

Efficient system design and component allocation have resulted in an unparalleled hardware flexibility. The basic processor, along with a sixteen register scratch-pad memory, occupy three standard PC modules (7½" X 7½"). Up to 2048 bytes of Read-Only Memory or 1024 bytes of Read-Write Memory are located on one standard module. This hardware allocation allows for complete memory interchangeability. Other options including interrupt logic, the index register, memory expansion logic, display panel control, and mag tape electronics are located on four standard boards. The CP-8 computers are available in the basic unpackaged form. Also, a 19 inch rack mounted enclosure or a decorative desk top enclosure is available.

ORGANIZATION

The basic CP-8 processor consists of six hardware arithmetic and logic registers, a binary adder and a memory. The registers perform the following functions:

- A— Accumulator, shifter, I/O buffer
- D— Data register, memory buffer
- F— Function register, contains code of currently executed function
- I— Index register or page register
- MA— Memory address register
- AS— Address storage register

The CP-8 is available with Read-Only Memory, Read-Write Memory and a Scratchpad Memory (up to 16 registers) or any combination of the three. Addressing is accomplished through the "MA" register for the program sequence and through the "I" register for the data indexing sequence. The "AS" register serves as an address storage register and facilitates subroutine exit. Arithmetic, logical, and data manipulation commands are performed in the "A" register and "K" link.

SPECIFICATIONS

- **Memory:** Read-Write — 1024 to 32K bytes;
1.5 microsecond cycle time
Read-Only — 512 to 4096 bytes;
350 nanoseconds cycle time
- **Word Size:** Byte Variable
- **I/O Data:** Byte parallel
- **Add Time:** 3.5 microseconds
- **I/O Logic Levels:** Standard I/C TTL logic levels
- **Power:** 115 volts \pm 10%, 50-60 HZ
- **Cabinet Size:** 19.75" wide X 21.67" deep X 7" high
- **Temperature:** 0° C to 45° C
- **Humidity:** 10% to 90% R. H.

CP-8

FAMILY INSTRUCTION SET

NEM DESCRIPTION

Accumulator (A) and Link (K) Control Instructions

NOP	No Operation
RR	Rotate Right A with K
RL	Rotate Left A with K
SR	Clear K; Rotate Right A with K
SL	Clear K; Rotate Left A with K
CRR	Complement K; Rotate Right A with K
CRL	Complement K; Rotate Left A with K
SRF	Set K; Rotate Right A with K
SLF	Set K; Rotate Left A with K
CLK	Clear K
STK	Set K
CPK	Complement K
PR1	Test Parity; Complement K if odd parity
PR2	Test Parity; Clear K if odd parity
PR3	Test Parity; Set K if odd parity
PR4	Test Parity; Complement K if even parity

Logical Instructions

LA	Load A immediate
CMP	Complement A
CLA	Clear A
FA	Fill A with Binary ones
•	AND A with memory; deposit in A
+	Inclusive OR A with memory; deposit in A

Arithmetic and Transfer Instructions

G	Get A from memory
S	Store A in memory
A	Add A to memory
AK	Add K to A
A+1	Increment A

NEM DESCRIPTION

Index (I) Control Instructions

IAI	Interchange A and I
IAS	Interchange I and address storage (AS) register
IA+	Interchange A and I; increment A
IAD	Interchange A and I; add K to A
IAR	Interchange A and I; rotate I four positions
RI	Rotate I four positions
LI	Load I immediate

Jump Instructions

JAO	Jump if A=0
JK1	Jump if K=1
JP	Jump
JS	Jump; store present address

Control Instructions

TPD	Take page from immediate byte
RET	Return address
RTI	Return address; enable interrupts
IOF	Interrupts off
ION	Interrupts on
STP	Stop

Input/Output Instructions

IN1	Conditional input from other processors
OT1	Conditional output to other processors
IN2	Unconditional input from peripherals
INC	Conditional input from peripherals
TST	Test peripherals
ACK	Acknowledge peripherals, output to peripherals

OPTIONS

- Up to 32 K bytes of Read-Write Memory
- Direct Memory access channel
- Up to 32 external interrupts available
- Real time clock
- Memory protection
- Memory parity
- Power failure protect
- Automatic restart

PERIPHERAL EQUIPMENT

The following Unicom peripheral equipment is currently available off-the-shelf.

- Page printer-featuring a 12 inch upper and lower case carriage and 10 characters per second capability
- ASCII keyboard
- Typewriter keyboard
- Alphanumeric ASCII display featuring a 400 character internal buffer (40 characters/line) capable of stand alone operation

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